REMARKS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1 and 4-29 are pending and under consideration.

I. Rejections under 35 U.S.C. § 103

In the Office Action, at pages 2-10, claims 15-17, 19-25, and 29 were rejected under 35 USC § 103(a) as being unpatentable over Yamada (U.S. Patent No. 5,950,222) in view of Iwata (U.S. Patent No. 5,881,295) and Computer Dictionary (Microsoft, "Computer Dictionary, Fifth Edition").

The Examiner concedes that Yamada does not disclose a conversion circuit. Specifically, Yamada does not discuss or suggest:

> a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag to convert the first address range to the second address range,

as recited in claim 15. The Examiner seeks to make up for this deficiency with reference to the address conversion circuit of Iwata (Iwata, col. 14, lines 6-15; col. 23, line 60 to col. 24, line 13; Fig. 5; Fig.19). However, Iwata does not discuss or suggest:

> a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag to convert the first address range to the second address range,

as recited in claim 15. In other words, the invention of claim 15 provides for a conversion circuit that *includes* both a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area. In contrast, Iwata, as relied on by the Examiner, does not disclose a conversion circuit that includes both a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a

second address range corresponding to the second storage area. The Examiner takes the position that registers PEREG and MBREG1 are analogous to the first pair of registers of claim 15 and that PEREG and MBREG2 are analogous to the second pair of registers of claim 15. However, this is submitted to be incorrect. PEREG, MBREG1, and MBREG2 are clearly disclosed as being part of control circuit FCONT, which is part of the flash memory, as clearly shown in Figs. 18-19 of Iwata. Therefore, Iwata does not disclose a first pair of registers and a second pair of registers within the conversion circuit. The conversion circuit of Iwata, shown in Fig. 5 and as relied on by the Examiner, does not include two pairs of registers, as is provided by the invention of claim 15. Furthermore, the program/erase control register and the erasing block designation registers of Iwata are *only* used by the control circuit of the flash memory for *erasing or programming the flash memory* (Iwata, col. 24, lines 15-18). Iwata makes no mention of the registers *setting a first address range* corresponding to the first storage area and *setting a second address range* corresponding to the second storage area, as is provided by the invention of claim 15. Computer Dictionary also fails to make up for these deficiencies in Yamada and Iwata.

Furthermore, the Examiner concedes that the combination of Yamada and Iwata does not disclose a second address range corresponding to a second, non-volatile storage area. The Examiner seeks to make up for this deficiency with reference to Computer Dictionary. The Examiner indicates that Computer Dictionary and the combination of Yamada and Iwata are analogous art because they are from the field of computer memory systems. This is submitted to be incorrect. Applicants respectfully submit that a dictionary defining terms relating to all fields of computers, including hardware, software, and peripherals, cannot be deemed to be in the field of computer memory systems. Computer Dictionary, as relied on by the Examiner, merely provides a definition for a non-volatile memory. The mere definition of the term "non-volatile memory" in a general computer dictionary is not sufficient motivation for one skilled in the art to have combined Computer Dictionary with Yamada and Iwata. Therefore, the motivation "to not lose data when power is removed from the memory device, thus decreasing the power consumption needed for data retention and also increasing system reliability during power loss," is not a proper motivation. Even if Computer Dictionary was combined with Yamada and Iwata, the invention of claim 15 would not result because Computer Dictionary *merely defines* a non-volatile memory.

Since the combination of Yamada, Iwata, and Computer Dictionary does not discuss or suggest all of the features of claim 15, and there is no proper motivation to combine the

references, claim 15 patentably distinguishes over the cited prior art. Accordingly, withdrawal of this § 103 (a) rejection is respectfully requested.

Claims 16-17 and 19-25 depend either directly or indirectly from claim 15, and include all the features of claim 15, plus additional features that are not discussed or suggested by the cited prior art. Therefore, claims 16-17 and 19-25 patentably distinguish over the cited prior art for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

The combination of Yamada, Iwata, and Computer Dictionary does not discuss or suggest:

> a conversion circuit that, based on a state of the flag, converts an address indicating a nonvolatile storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a nonvolatile storage place of a corresponding alternate interrupt vector,

as recited in claim 29. Therefore, claim 29 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

In the Office Action, at pages 10-15, claims 1, 4, and 6-12 were rejected under 35 USC § 103(a) as being unpatentable over Yamada in view of Iwata, Hashimoto (U.S. Patent No. 6,654,839), and Computer Dictionary.

As discussed above, the combination of Yamada, Iwata, and Computer Dictionary does not discuss or suggest:

> a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address,

as recited in claim 1. Hashimoto fails to make up for this deficiency. Specifically, Hashimoto does not discuss or suggest:

> a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of

> the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address,

as recited in claim 1. Therefore, claim 1 patentably distinguishes over Yamada, Iwata, Computer Dictionary and Hashimoto. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 4 and 6-12 depend either directly or indirectly from claim 1, and include all the features of claim 1, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 4 and 6-12 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

In the Office Action, at pages 15-19, claim 28 was rejected under 35 USC § 103(a) as being unpatentable over Yamada in view of Iwata, Yoshioka et al. (U.S. Patent No. 6,038,661) and Computer Dictionary.

As discussed above, combination of Yamada, Iwata, and Computer Dictionary does not discuss or suggest:

> a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by adding the offset to the first address,

as recited in claim 28. Yoshioka et al. fails to make up for this deficiency. Specifically, Yoshioka et al. does not discuss or suggest:

> a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by adding the offset to the first address,

as recited in claim 28. Therefore, claim 28 patentably distinguishes over Yamada, Iwata, Computer Dictionary, and Hashimoto. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

In the Office Action, at pages 15-19, numbered paragraphs 27-34, claims 5, 13-14, 18, and 26-27 were rejected under 35 USC § 103(a) as being unpatentable over Yamada in view of Iwata and Computer Dictionary and further in view of various other combinations of prior art. None of the cited prior art makes up for the deficiencies noted above.

Claims 5 and 13-14 and claims 18 and 26-27 depend either directly or indirectly from claims 1 and 15, respectively, and include all the features of claims 1 and 15, plus additional features that are not discussed or suggested by the cited prior art. Therefore, claims 5, 13-14, 18, and 26-27 patentably distinguish over the cited prior art for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

II. Interview Request

Applicant respectfully requests a telephone interview between Applicant's representative, the undersigned, and the Examiner at the Examiner's earliest convenience, in order to discuss the arguments presented in the current response. The undersigned can be reached by telephone directly at (202) 454-1583.

III. IDS Filed August 21, 2007

Applicant respectfully requests entry and consideration of the IDS filed on August 21, 2007.

CONCLUSION

Claims 1 and 4-29 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 10-31-07

By: _____

Aaron C. Walker
Registration No. 59,921

1201 New York Avenue, N.W., 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501